SIGMA-DELTA MODULATOR AND FRACTIONAL-N FREQUENCY SYNTHESIZER COMPRISING SAME

BACKGROUND OF THE INVENTION

5

1. Technical Field

The present disclosure relates to a sigma-delta ($\Sigma - \Delta$) modulator and a fractional-N frequency synthesizer comprising same, and more particularly, to a multi-bit multiple-order interpolative $\Sigma - \Delta$ modulator and a fractional-N

10 phase-locked loop (PLL) frequency synthesizer comprising the same.

2. Discussion of the Related Art

PLL frequency synthesizers synthesize desired signals using a reference signal and control a ratio of the synthesized signal to the reference signal using a controller.

15 PLL frequency synthesizers may employ an integer-N technique and a fractional-N technique. The integer-N technique uses a fixed integer N to divide an output frequency, and the fractional-N technique uses a number N to divide the output frequency which is selected among two or more integers (e.g., N is varied between two or more integers such that the average value of N is fractional). As a

20 result, a divisor is fractional when using the fractional-N technique due to interpolation of each number N selected for every dividing operation.

It may be difficult to meet certain specifications when employing the integer-N technique due to a trade-off between loop bandwidth and channel spacing, while the fractional-N technique alleviates design restrictions on PLLs permitting a broader

25 loop bandwidth while maintaining narrow channel intervals.

The $\Sigma - \Delta$ modulator provides a control signal necessary for selecting N in the fractional-N technique.

The $\Sigma - \Delta$ modulator may be classified as a multistage-noise-shaping (MASH) $\Sigma - \Delta$ modulator and an interpolative $\Sigma - \Delta$ modulator. As shown in FIG.

30 1, a first-order MASH $\Sigma - \Delta$ modulator forms an independent loop and is cascaded to another loop in order to construct a high-order modulator. Thus, the high-order modulator can be unconditionally stable and use most of an input range. However, the overall structure of the high-order modulator is complicated. The cascaded first-order modulator causes poor idle-tone characteristics. In order to improve the

idle-tone characteristics, each node must vary an output signal of the MASH $\Sigma - \Delta$ modulator by using an independent dither that does not affect another node.

When the MASH $\Sigma - \Delta$ modulator is a multi-bit modulator, a pass-band gain level of the multi-bit modulator is high, resulting in output value changes over a large range. Accordingly, in a fractional-N frequency synthesizer using the MASH $\Sigma - \Delta$ modulator, a non-linear error in a phase/frequency detector increases with an increase of the range of output value changes, thereby greatly limiting the performance of the fractional-N frequency synthesizer.

The interpolative $\Sigma - \Delta$ modulator has a structure as shown in FIG. 2. The structure of the interpolative $\Sigma - \Delta$ modulator is simpler than that of the MASH $\Sigma - \Delta$ modulator. In addition, when the interpolative $\Sigma - \Delta$ modulator is used as a multi-bit modulator, the interpolative $\Sigma - \Delta$ modulator has a lower pass-band gain level than the MASH $\Sigma - \Delta$ modulator, resulting in output value changes over a smaller range than with a MASH $\Sigma - \Delta$ modulator.

In consideration of the above, a fractional-N frequency synthesizer using a single-bit 4th-order $\Sigma - \Delta$ modulator has been proposed. The single-bit 4th-order $\Sigma - \Delta$ modulator is not as stable as the MASH $\Sigma - \Delta$ modulator and thus guarantees stability over only a limited input range. In other words, a dead band occurs over the full input range. As a result, as shown in FIG. 3, the single-bit 4th-order $\Sigma - \Delta$ modulator uses only 50% of the full input range and maps an output value into N-1 or N+1. This results in 1 bit loss and an increase in quantization noise by 6dB.

In addition, a quantization noise transfer function of the single-bit 4th-order $\Sigma - \Delta$ modulator functions like a high-pass filter. When the single-bit 4th-order $\Sigma - \Delta$ modulator is of an interpolative type, a pass band gain level must be less than a threshold in order to maintain stability. The pass band gain level is generally adjusted using a Butterworth filter coefficient. Since a total amount of the quantization noise is maintained at a constant level, the threshold in order to maintain stability and a corner frequency of the pass band gain level show a trade-off tendency as seen in FIG. 4. In other words, the pass band gain level increases when the corner frequency increases, and the pass band gain level decreases when the corner frequency decreases.

When f_s is an operation frequency, the maximum corner frequency that guarantees the stability of the single-bit 4th-order $\Sigma - \Delta$ modulator is 0.06(f_s). FIGS.

5A and 5B respectively show a quantization noise transfer curve of the single-bit 4th-order $\Sigma - \Delta$ modulator and the output of a PLL with respect to frequency. In FIG. 5B, slanted line 60 denotes out-of-band phase noise of a voltage controlled oscillator (VCO) of the PLL. As can be seen in FIG. 5B, phase noise of the PLL

5   becomes increasingly worse when the frequency approaches the corner frequency of the single-bit 4th-order $\Sigma - \Delta$ modulator.

Lastly, the single-bit 4th-order $\Sigma - \Delta$ modulator without dithering causes unwanted idle-tones. FIG. 6 shows the result of autocorrelation for 2000 outputs of the single-bit 4th-order $\Sigma - \Delta$ modulator. As can be seen in FIG. 6, the

10   autocorrelation results vary within a large range.

Accordingly, there is a need for a $\Sigma - \Delta$ modulator and a stable fractional-N frequency synthesizer using the $\Sigma - \Delta$ modulator.

SUMMARY OF THE INVENTION

15

A fractional-N frequency synthesizer, according to an embodiment of the present invention, includes a phase detector, a voltage controlled oscillator, a divider, and a sigma-delta modulator. The phase detector detects a phase difference between a reference signal and a feedback signal. The voltage controlled oscillator

20   receives a phase difference control signal based on the detected phase difference and oscillates a signal with a frequency based on the detected phase difference. The divider selects a value from at least three integers according to a predetermined selection signal, divides the frequency of the oscillated signal output from the voltage controlled oscillator by the selected value, and outputs a divided signal as a

25   feedback signal to the phase detector. The sigma-delta modulator adds a predetermined input value to an internal feedback value, successively accumulates added values, quantizes the an accumulated value to at least three levels, and converts a quantized value into the predetermined selection signal.

The sigma-delta modulator may include a plurality of operation units for

30   adding the predetermined input value to the internal feedback value and for successively accumulating the added values, a quantizer for quantizing the accumulated value output from a last one of the plurality of operation units to a plurality of bits and for outputting the quantized value as the predetermined selection signal to the divider, and a plurality of multipliers for outputting feedback coefficients

as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits. The feedback coefficients may be symmetrical values spaced at equal intervals around a middle level of the at least three levels. The feedback

5   coefficients may be converted into bit streams with binary values. The fractional-N frequency synthesizer may further include a control signal generator for receiving a plurality of bit values output from the quantizer and for outputting a minimum number of control signals depending on symmetrical values of the bit streams. The control signal generator may include a gray coder for converting the plurality of bit values

10   into a gray code, a plurality of control signal generating units for receiving the gray code and for outputting the control signals, a plurality of inverters for inverting outputs of the plurality of control signal generating units. The multipliers may include connections for outputting the bit streams from the control signals of the control signal generator directly to the plurality of operation units.

15   A sigma-delta modulator, according to an embodiment of the present invention, includes a plurality of operation units, a quantizer, and a plurality of multipliers. The plurality of operation units add input values to internal feedback values and successively accumulate the added values up to a fourth order. The quantizer quantizes an accumulated value output from a last one of the plurality of

20   operation units into a plurality of bits. The plurality of multipliers output feedback coefficients as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits.

The feedback coefficients may be symmetrical values spaced at equal

25   intervals around a middle level of a plurality of levels output from the quantizer. The feedback coefficients may be converted into bit streams with binary values. The sigma-delta modulator may further include a control signal generator for receiving a plurality of bit values output from the quantizer and for outputting a minimum number of control signals depending on symmetrical values of the bit streams. The control

30   signal generator may include a gray coder for converting the plurality of bit values into a gray code, a plurality of control signal generating units for receiving the gray code and for outputting the control signals, and a plurality of inverters for inverting outputs of the control signal generating units. The multipliers may include

4

connections for outputting the bit streams from the control signals of the control signal generator directly to the plurality of operation units.

A frequency synthesizer, in accordance with an embodiment of the present invention, includes a phase detector for detecting a phase difference between a reference signal and a feedback signal, a voltage controlled oscillator for receiving a phase difference control signal based on the detected phase difference, and for outputting a signal with a frequency based on the detected phase difference, a divider for selecting a value from a plurality of integers according to a predetermined selection signal, for dividing the frequency of the signal output from the voltage controlled oscillator by the selected value, and for outputting a divided signal as a feedback signal to the phase detector, and a modulator for adding a predetermined input value to an internal feedback value, for successively accumulating added values, for quantizing an accumulated value to a plurality of levels, and for converting a quantized value into the predetermined selection signal.

The modulator may include a plurality of operation units for adding the predetermined input value to the internal feedback value and for successively accumulating the added values, a quantizer for quantizing the accumulated value output from a last one of the plurality of operation units to a plurality of bits and for outputting the quantized value as the predetermined selection signal to the divider, and a plurality of multipliers for outputting feedback coefficients as internal feedback values to each of the plurality of operation units, wherein the feedback coefficients are determined according to a quantized level corresponding to the plurality of bits.

The feedback coefficients may be symmetrical values spaced at equal intervals around a middle level of the plurality of levels.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention can be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings in which:

FIG. 1 shows the configuration of a typical MASH $\Sigma - \Delta$ modulator;

FIG. 2 shows the configuration of a typical interpolative $\Sigma - \Delta$ modulator;

FIG. 3 shows an input range and mapping of output values of a single-bit 4th-order $\Sigma - \Delta$ modulator;

FIG. 4 shows the relationship between a corner frequency for a quantization noise transferfunction and a pass band gain level;

FIG. 5A shows the quantization noise transfer curve of the single-bit 4th-order $\Sigma - \Delta$ modulator referred to in FIG. 3;

FIG. 5B shows the output phase noise of a PLL of the single-bit 4th-order $\Sigma - \Delta$ modulator referred to in FIG. 3;

FIG. 6 shows autocorrelation results of the single-bit 4th-order $\Sigma - \Delta$ modulator referred to in FIG. 3;

FIG. 7 is a block diagram of a fractional-N frequency synthesizer according to an embodiment of the present invention;

FIG. 8A is a block diagram of a 3-bit 4th-order $\Sigma - \Delta$ modulator according to an embodiment of the present invention;

FIG. 8B is a block diagram of a control signal generator shown in FIG. 8A;

FIG. 9 shows an input range and mapping of output values of the 3-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A;

FIG. 10A shows a quantization noise transfer curve of the 3-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A;

FIG. 10B shows output phase noise of a PLL of the 3-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A; and

FIG. 11 shows autocorrelation results of the 3-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described more fully hereinafter below in more detail with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

FIG. 7 is a block diagram of a fractional-N frequency synthesizer according to am embodiment of the present invention. Referring to FIG. 7, the fractional-N frequency synthesizer has a feedback loop which divides an output signal f_{out} of the fractional-N frequency synthesizer and then outputs a phase control signal f_d. The

division of the output signal f_{out} is achieved by a divider 13 and a $\Sigma - \Delta$ modulator 14 which controls a division ratio of the divider 13. The divider 13 divides the output signal f_{out} using a value that is selected from three or more integers in accordance with a selection signal output from the $\Sigma - \Delta$ modulator 14. It is preferable that the

5   $\Sigma - \Delta$ modulator 14 is a multi-bit multiple-order $\Sigma - \Delta$ modulator, which will be described in connection with FIG. 8A.

The phase control signal f_d is input to a phase detector (PD) 10 and then compared with a reference signal f_{ref}. The PD 10 outputs a control signal with a direct current voltage proportional to a phase difference between the phase control

10 signal f_d and the reference signal f_{ref}. The control signal passes through a low-pass filter (LPF) 11 and then is input to a voltage controlled oscillator (VCO) 12. The VCO 12 then outputs the output frequency f_{out} according to the control signal input into the VCO 12.

FIG. 8A is a block diagram of a 3-bit 4th-order $\Sigma - \Delta$ modulator according to

15 an embodiment of the present invention. Referring to FIG. 8A, the 3-bit 4th-order $\Sigma - \Delta$ modulator includes a first operation unit 80, a second operation unit 81, a third operation unit 82, a fourth operation unit 83, a 3-bit quantizer 84, and a control signal generator 85. The first operation unit 80 includes a feedback coefficient multiplier 801, an adder 802, an accumulator (ACC) 803, and a dynamic scaling

20 coefficient multiplier 804. The ACC 803 may include an adder (not shown) and a delayer (not shown) which are interconnected. Similarly, the second, third and fourth operation units each include a feedback coefficient multiplier 811, 821 and 831, an adder 812, 822 and 832, and an accumulator (ACC) 813, 823 and 833. The second and third operation units 81 and 82 each include a dynamic scaling

25 coefficient multiplier 814 and 824.

The operation of the 3-bit 4th-order $\Sigma - \Delta$ modulator will now be explained. The first, second, third, and fourth operation units 80, 81, 82, and 83 perform in a similar manner. Thus, only the behavior of the first operation unit 80 will be described herein. The feedback coefficient multiplier 801 determines one out of 8

30 feedback coefficients by combining control signals generated from outputs of the 3-bit 4th-order $\Sigma - \Delta$ modulator and then outputs the determined feedback coefficient to the adder 802. The adder 802 adds the determined feedback coefficient to a frequency control value input within an input range. The ACC 803 accumulates values output from the adder 802, and the dynamic scaling coefficient

7

multiplier 804 multiplies an accumulated value by a dynamic scaling coefficient. The addition and accumulation are also performed in the second, third and fourth operation units 81, 82 and 83. After performing addition and accumulation in the fourth operation unit 83, the 3-bit quantizer 84 quantizes a resulting accumulated

5   value output from the fourth operation unit 83 to a plurality of levels. The quantized value is output to the divider 13 and then output as a selection signal for selecting one from 8 output values ranging from N-3 to N+4. If a 2- or 4- bit quantizer is used, the divider 13 selects 4 or 16 values, i.e., one from 2^n values, where n is 2 or 4.

       The quantized value is also input to the control signal generator 85, and the

10   control signal generator 85 generates control signals which are provided to the feedback coefficient multipliers 801, 811, 821, and 831 of the first, second, third, and fourth operation units 80, 81, 82, and 83, respectively.

       With the 3-bit 4th-order $\Sigma - \Delta$ modulator, the number of output values increases to 8 levels which are mapped from N-3 to N+4 as shown in FIG. 9. Thus,

15   although only 1/8 of the full input range may be used, the output level can be mapped to N or N+1. In addition, quantization noise is attenuated, resulting in a higher corner frequency.

       Compared to single-bit quantization, 3-bit quantization reduces quantization noise by 1/8. FIG. 10A shows a quantization noise transfer curve of the 3-bit

20   4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A. As can be seen in FIG. 10A, the corner frequency of the 3-bit 4th-order $\Sigma - \Delta$ modulator is increased by double or more from of the single-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 5A. FIG. 10B shows output phase noise of a PLL of the 3-bit 4th-order $\Sigma - \Delta$ modulator shown in FIG. 8A. Unlike in the single-bit 4th-order $\Sigma - \Delta$ modulator, phase noise of the PLL

25   of the 3-bit 4th-order $\Sigma - \Delta$ modulator does not surpass the slanted line 60 denoting out-of band phase noise, which results in improved out-of-band phase noise characteristics.

       Referring to FIG. 11, when compared with the single-bit 4th-order $\Sigma - \Delta$ modulator, the three-bit 4th-order $\Sigma - \Delta$ modulator shows improved idle-tone

30   characteristics. FIG. 11 shows the autocorrelation results for 2000 output samples of the 3-bit 4th-order $\Sigma - \Delta$ modulator. The output range of autocorrelation of the 2000 output samples is reduced to about 1/10 of that shown in FIG. 6.

       When constructing the 3-bit 4th-order $\Sigma - \Delta$ modulator,. since scaling coefficients can be generally realized in the form of the square of 2, the dynamic

scaling coefficient multipliers 804, 814, and 824 can be realized through simple shifters.Further, as an alternative to using the feedback coefficient multipliers 801, 811, 821, and 831, the feedback coefficients may be stored in a read-only memory (ROM). As a result, whenever necessary, corresponding feedback coefficients can

5   be read from the ROM to be output to adders 802, 812, 822, and 832 of the operation units 80, 81, 82, and 83, respectively. When storing the feedback coefficients in a ROM device, a ROM medium capable of storing 32 coefficients is preferred because, in a case of 3-bit output, the feedback values are input to each of the logic units 80, 81, 82, and 83 over four paths and it can be burdensome to select

10   one coefficient from 8 coefficients. Accordingly, a ROM medium to store 32 coefficients is preferred, and a total capacity of 640 bits of ROM is preferred, while a 20-bit register is used for one coefficient. Thus, multipliers may also be realized through only metallic connections, thereby reducing the amount of hardware used.

Table 1 below shows outputs of the 3-bit quantizer 84, expressed as

15   normalized feedback coefficients at equal intervals (e.g., 0.250) in order to realize the multipliers through only metallic connections.

[Table 1]

coefficient 1	0.875
coefficient 2	0.625
coefficient 3	0.375
coefficient 4	0.125
coefficient 5	-0.125
coefficient 6	-0.375
coefficient 7	-0.625
coefficient 8	-0.875

20   Table 2 below shows 20-bit feedback coefficient example which may be provided to each operation unit 80, 81, 82 and 83.

Bit Group	20		19	18	17	16	15							5	4	3	2	1
Coefficient 1	0		0	1	0	1	0		.	.	.	.	.		0	1	0	0	0
Coefficient 2	0		0	0	1	1	1		.	.	.	.	.		0	1	0	0	0
Coefficient 3	0		0	0	1	0	0		.	.	.	.	.		1	1	0	0	0
Coefficient 4	0		0	0	0	0	1		.	.	.	.	.		1	1	0	0	0
Coefficient 5	1		1	1	1	1	0		.	.	.	.	.		0	1	0	0	0
Coefficient 6	1		1	1	0	1	1		.	.	.	.	.		0	1	0	0	0
Coefficient 7	1		1	1	0	0	0		.	.	.	.	.		1	1	0	0	0
Coefficient 8	1		1	0	1	0	1		.	.	.	.	.		1	1	0	0	0

In Table 2, since one feedback coefficient is expressed with 20 bits, 2^{20} bit combinations are possible. However, each bit group, which represents 8 feedback coefficients at the same time, is expressed with 8 bits and thus has 2^8 available bit combinations. In accordance with an embodiment of the present invention, 8 feedback coefficients in each operation unit may be simultaneously expressed through combinations of bit groups and, thereby mimimizing a number of combinable signals of bit groups and the amount of hardware used.

As can be seen in Table 2, first through fourth bit groups each contain coefficients 1 through 8 with equal bit values, and fifth through twelfth bit groups each contain coefficients 1 through 8, in which coefficients 5 through 8 have inverted bit values with respect to bit values of coefficients 4 through 1. The inversion of bit values is due to the expression of feedback coefficients through the conversion of a value output from the 3-bit quantizer 84 into a symmetrical gray code signal. As a result, a number of signals of available bit groups is 2^4 according to the symmetrical characteristic.

When the above characteristic is realized into hardware, for bit groups with equal bit values, the values of "0" or "1" are connected directly to the adder 802, 812, and 822. For bit groups with inverted bit values, control signals generated from outputs of the 3-bit quantizer 84, which exhibit the inversion characteristic shown in Table 2, are input directly to the adder 802, 812, and 822, respectively, through metallic connections.

When describing the bit groups with inverted bit values, a total of 16 control signals may be generated, of which 8 control signals are inverted with respect to the remaining 8 control signals. Thus, in a case where the control signal generator 85

converts a value output from the 3-bit quantizer 84 into gray code data to make 8 control signals, the feedback coefficient multipliers 801, 811, 821, and 831 can be realized only through metallic connections so that the amount hardware used is minimized. A 3-bit quantizer 84 requires 8 control signals. Alternatively, a 2-bit

5   quantizer requires 2 control signals and a 4-bit quantizer requires 128 control signals.

FIG. 8B is a block diagram of the control signal generator 85. Referring to FIG. 8B, the control signal generator 85 includes a gray coder 850, a plurality of control signal generating units 851, and a plurality of inverters 852.

10   The gray coder 850 converts the output from the 3-bit quantizer 84 into the gray code data. Since the control signal generating units 851 include a variety of logic units, such as AND gates and the like, they receive the gray code data, and output a portion of the results as shown in Table 2 via the inverters 852. Accordingly, the control signal generator 85 can generate 8 control signals from a

15   3-bit output of the 3-bit quantizer 84. In addition, the control signal generator 85 can contribute to the realization of the feedback coefficient multipliers 801, 811, 821, and 831, and the dynamic scaling coefficient multipliers 804, 814, and 824 through only metallic connections by combining the 8 control signals and the inverted signals according to Table 2.

20   As described above, a single-bit modulator can be configured into a multi-bit modulator. When compared to the single-bit modulator, the multi-bit modulator enables a usable input range to be reduced and output levels to be increased. As a result, only 1/8 of the full input range of the multi-bit modulator is needed to map an output level to N or N+1. In addition, the multi-bit modulator can reduce quantization

25   noise and thus allow a corner frequency to be higher. Moreover, increases in hardware can be minimized by realizing multipliers through only metallic connections.

Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present

30   invention is not limited to those precise embodiments, and that various other changes and modifications may be affected therein by one of ordinary skill in the related art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.